

FDMB506P

P-Channel 1.8V Logic Level PowerTrench® MOSFET

General Description

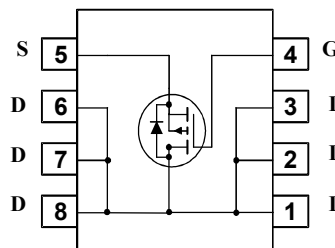
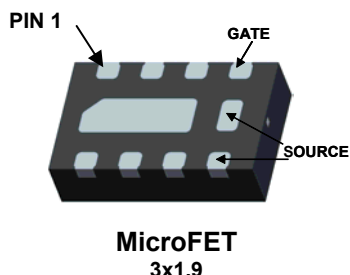
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for portable electronics applications.

Applications

- Load switch
- DC/DC Conversion

Features

- -6.8 A, -20V. $R_{DS(ON)} = 30\text{ m}\Omega @ V_{GS} = -4.5\text{V}$
 $R_{DS(ON)} = 38\text{ m}\Omega @ V_{GS} = -2.5\text{V}$
 $R_{DS(ON)} = 70\text{ m}\Omega @ V_{GS} = -1.8\text{V}$
- Low profile – 0.8 mm maximum
- Fast switching
- RoHS compliant



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	-20	V
V _{GSS}	Gate-Source Voltage	±8	V
I _D	Drain Current – Continuous (Note 1a)	-6.8	A
	– Pulsed	70	
P _D	Power Dissipation (Note 1a)	1.9	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	65	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1b)	208	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
506	FDMB506P	7"	8mm	3000 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		-13		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.7	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -6.8\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -2.5\text{ A}$ $V_{GS} = -1.8\text{ V}, I_D = -1.8\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -6.8\text{ A}, T_J = 125^\circ\text{C}$		25 30 40 36	30 38 70 44	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -6.8\text{ A}$		26		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$		2216	2960	pF
C_{oss}	Output Capacitance	$f = 1.0\text{ MHz}$		351	470	pF
C_{rss}	Reverse Transfer Capacitance			167	260	pF

Switching Characteristics (Note 2)

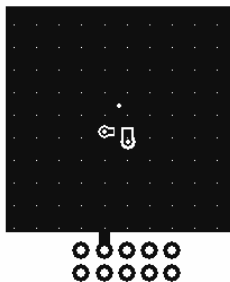
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$		14	25	ns
t_r	Turn–On Rise Time	$V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			175	280	ns
t_f	Turn–Off Fall Time			80	128	ns
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -6.8\text{ A},$		21	30	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = -4.5\text{ V}$		3.5		nC
Q_{gd}	Gate–Drain Charge			4.5		nC

Drain–Source Diode Characteristics and Maximum Ratings

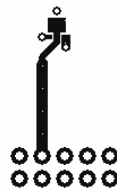
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.6	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.8\text{ A}$ (Note 2)		-0.6	-1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -6.8\text{ A},$		26	48	nS
Q_{rr}	Diode Reverse Recovery Charge	$dI_F/dt = 100\text{ A}/\mu\text{s}$		12	22	nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper

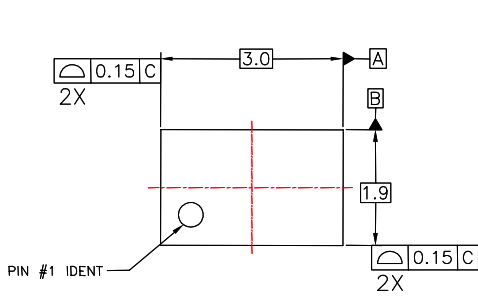


b) 160°C/W when mounted on a minimum pad of 2 oz copper

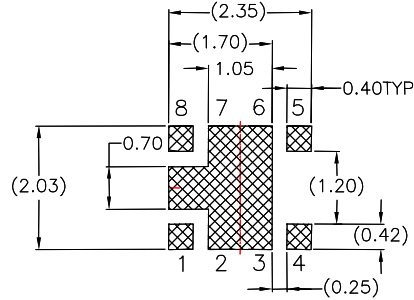
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\ \mu\text{s}$, Duty Cycle < 2.0%

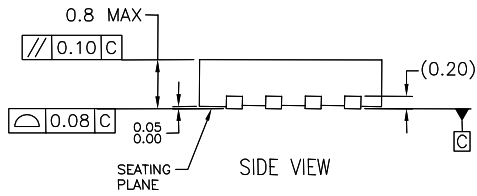
Dimensional Outline and Pad Layout



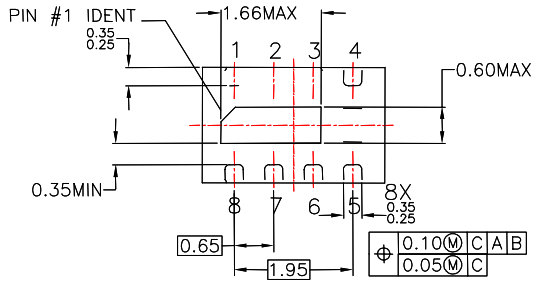
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

Typical Characteristics

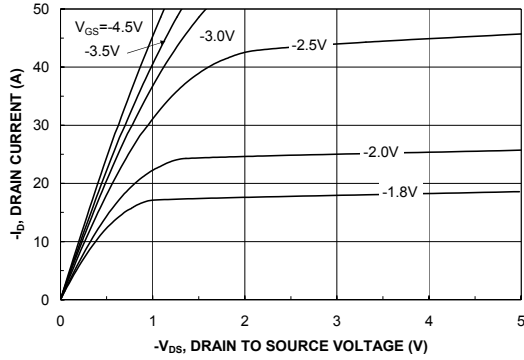


Figure 1. On-Region Characteristics.

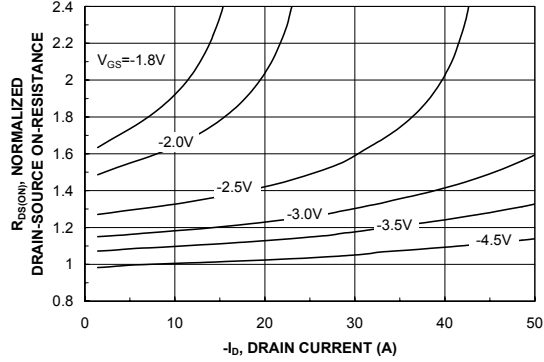


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

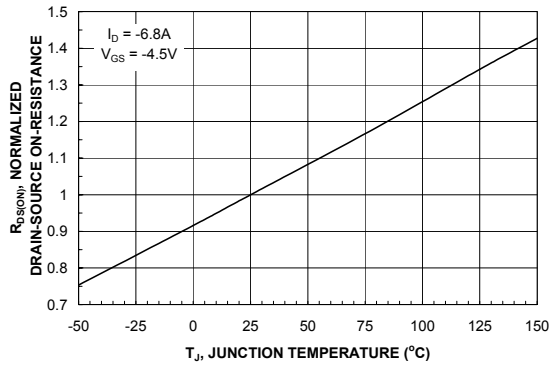


Figure 3. On-Resistance Variation with Temperature.

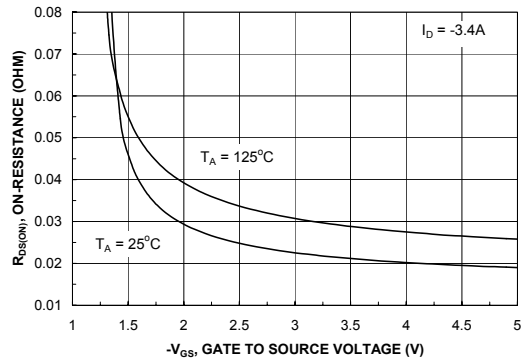


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

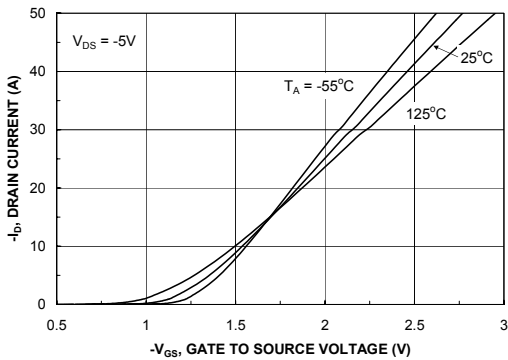


Figure 5. Transfer Characteristics.

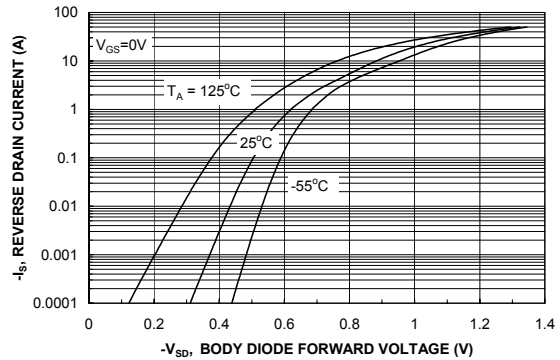


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

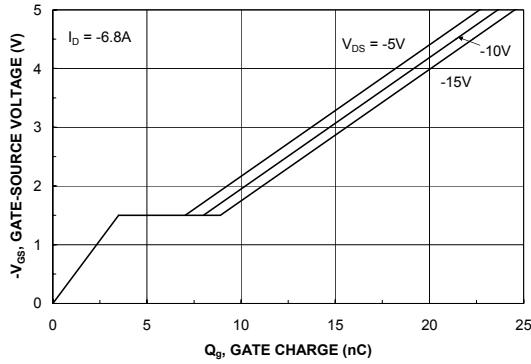


Figure 7. Gate Charge Characteristics.

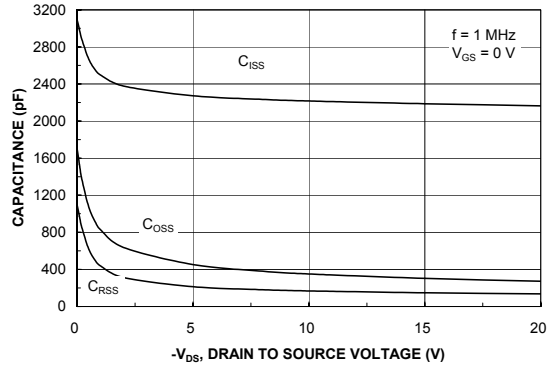


Figure 8. Capacitance Characteristics.

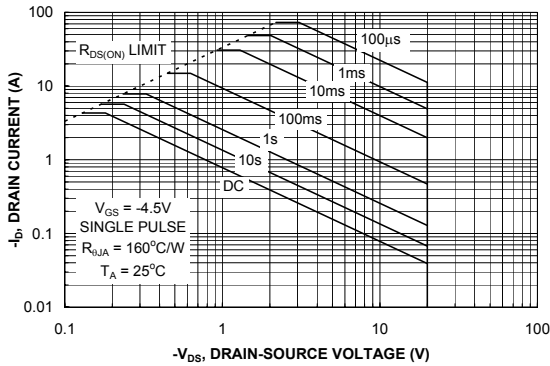


Figure 9. Maximum Safe Operating Area.

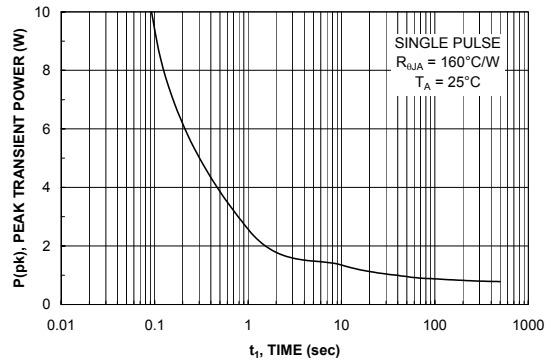


Figure 10. Single Pulse Maximum Power Dissipation.

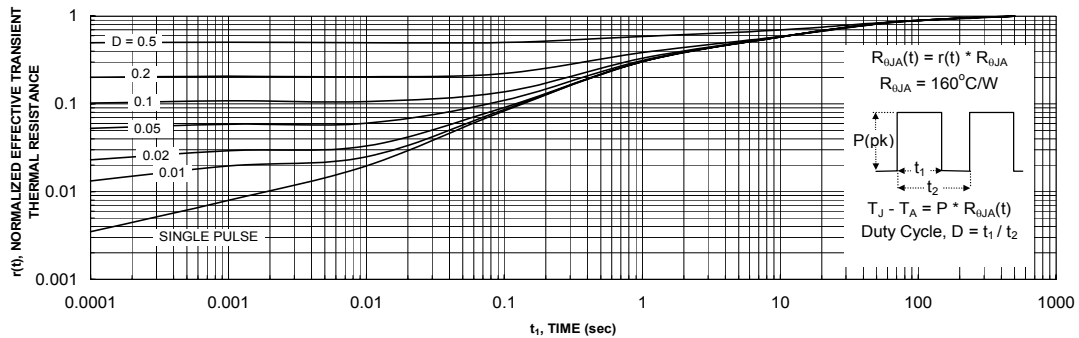


Figure 9. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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